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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/055,402	01/25/2002	Hiroki Satoh	016907-1365	7246

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EXAMINER	
PATEL, KANJIBHAI B	
ART UNIT	**PAPER NUMBER**
2625	

DATE MAILED: 01/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/055,402	SATOH, HIROKI	
	Examiner	Art Unit	
	Kanji Patel	2625	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 January 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5-14 and 16-19* is/are rejected.

7)☒ Claim(s) *4,15* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 January 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1/25/02*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. Drawings filed on 1/25/02 have been approved by the examiner.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-3, 6, 10, 12-14 and 17 are rejected under 35 U.S.C. 102(b) as being anticipated by Paik et al. (referred to as Paik) (US 6,163,621).

For claim 1, representative of claims 10 and 12, Paik discloses an equalizing circuit (column 8, lines 39-41 and more particularly 88 in figure 4 is a equalized value generating unit) comprising:

a memory control unit (102 in figure 4 controls input image data storage unit 80), which receives an input of an input image data signal;

a register setting unit which receives setting of a main scan coordinate and a subscan coordinate to start at least the equalizing of the input image data signal (column 3 line 49 to column 4 line 41; step 10 in figure 1 is used to set an arbitrary window of size P and Q for starting the equalization process in main scan direction and subscan direction);

an equalizing control unit which starts the equalizing of the input image data signal from the main scan coordinate and the subscan coordinate, which are set by the register setting unit, and outputs the equalized image data signal (col. 4, lines 42-67);

an output control unit (controller 102 in figure 4 controls equalized output values stored in storage unit 140 by signal C5) which receives an input of an equalized image data signal from the equalizing control unit and outputs it as an output image data signal (figure 1, step 30 is a equalized output).

For claim 2, Paik discloses an equalizing circuit wherein the register setting unit receives setting with respect to a size of an equalized block as an unit for equalizing the input image data (column 4, lines 1-41; step 10 is used to set a window size which corresponds to a block).

For claims 3 and 14, Paik discloses an equalizing circuit wherein the register setting unit receives setting of a skew value (column 4, lines 17-26; offset values as shown in figure 3A provides a skew value) of an equalized block as a unit for equalizing the input image data.

For claims 6 and 9, Paik discloses an equalizing circuit, wherein the equalizing control unit further has an equalized matrix generating/calculating circuit (steps 10, 12; figure 1; column 4, lines 1-26), which is used in common independently of a size of the equalized block.

For claim 13, Paik discloses an equalizing method wherein, when the register setting unit receives setting with respect to a size of an equalized block as an unit for equalizing the input image data, the equalizing control unit performs the equalizing on

the basis of the present equalized block (column 4, lines 1-41; step 10 is used to set a window size which corresponds to a block).

For claim 17, Paik discloses an equalizing method wherein the equalizing control unit (102, 88) sets an equalized block as an unit of the equalizing by a certain mode signal (column 11, lines 7-30; a sequence of operation reads on providing certain mode).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 5, 7-9, 11, 16 and 18-19 are rejected under 35 U>S.C. 103(a) as being unpatentable over Paik et al. (referred to as Paik) (US 5,163,621) as applied to claims 1-3, 6, 8-14, 17 and 19 above and further in view of Chang et al. (referred to as Chang) (US 6,385,101 B1).

For claims 5, 7, 16 and 18, Paik reference does not provide the use of delay predetermined delay for the input data as claimed. Chang discloses a programmable delay control for sense amplifiers in a memory (title). Paik further discloses the delay adjustment circuitry 32, 80 as shown in figures 1 and 2 and a predetermined delay as shown in figure 3 controlled by the memory control blocks. It would have been obvious to modify Paik by incorporating the delay and predetermined delay for the input image

data. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Paik by the teaching of Chang because he provides a programmable delays within the block control circuits, such as delay adjust circuit 40 that is within block control circuit 21, are programmed to have same delay as shown by Chang in column 6, lines 45-50.

For claim 8, Paik discloses an image processing circuit (figures 1, 4) comprising:

a memory control unit which receives an input of an input image data signal (see figure 4, controller 102, IN2);

a first memory which stores the input image data **signal** (80);

a CPU (figure 4, 102 acts as a CPU) which designates at least any one of a main scan coordinate and a subscan coordinate to start equalizing of the input image data signal, a main scan size and a subscan size of the equalized block and skew values in a main scan direction and in a subscan direction of the equalized block (controller 102 in figure 4 designates the window having main scan coordinates and subscan coordinates represented by the pixels of the window in columns and rows; see also figure 1; all steps are performed by the control unit);

a register setting unit which holds the setting information which is designated by the CPU (controller 102 provides a setting for storage);

an equalizing control unit which performs the equalizing of the input image data signal at certain timing independently of a skew value of the equalized block on the basis of the setting information held by the register setting unit and outputs the equalized image data signal (col. 4, lines 42-67);

a second memory (100 in figure 4 is a second memory) which receives an input of the equalized image data signal from the equalizing control unit and holds it as an output image data signal; and

an output control unit (102 in figure 4) which outputs the output image data of the second memory.

Paik reference does not provide the use of delay for the input data as claimed. Chang discloses a programmable delay control for sense amplifiers in a memory (title). Paik further discloses the delay adjustment circuitry 32, 80 as shown in figures 1 and 2 and a predetermined delay as shown in figure 3 controlled by the memory control blocks. It would have been obvious to modify Paik by incorporating the delay and predetermined delay for the input image data. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Paik by the teaching of Chang because he provides a programmable delays within the block control circuits, such as delay adjust circuit 40 that is within block control circuit 21, are programmed to have same delay as shown by Chang in column 6, lines 45-50.

For claims 11 and 19, see the rejection of claim 8 above.

For claim 9, Paik discloses an image processing circuit wherein the equalizing control unit further has an equalized matrix generating/calculating circuit which is used in common independently of a size of the equalized block (figures 3A-3B).

Allowable Subject Matter

4. **Claims 4 and 15** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Other prior art cited

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Lewins et al. (US 5,640,469) discloses a systems and methods for producing high-contrast, intensity equalized visible images.

Menkhoff (US 5,714,918) discloses an equalizer for digitized signals.

Bottomley et al. (US 5,577,068) disclose a generalized direct update viterbi equalizer.

Strolle et al. (US 5,835,532) disclose a blind equalizer for a vestigial sideband signal.

Chon (US 6,222,782 B1) discloses a control circuit for a bit line equalization signal I semiconductor memory.

Torpie et al. (US 3,798,576) disclose an automaitic equalization method and apparatus.

Contact Information

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kanji Patel whose telephone number is (703) 305-4011. The examiner can normally be reached on Monday to Thursday from 8:00 a.m. to 6:30 p.m. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bhavesh Mehta, can be reached on (703) 308-5246. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Kanji Patel
Art Unit 2625
January 6, 2004

KANJIBHAI PATEL
PRIMARY EXAMINER